SYNCHRONIZED MULTI-OUTPUT DIGITAL CLOCK MANAGER

John D. Logue
Andrew K. Percey
F. Erich Goetting

ABSTRACT OF THE DISCLOSURE

A digital clock manager is provided. The digital clock manager generates an output clock signal that causes a skewed clock signal to be synchronized with a reference clock signal. Furthermore, the digital clock manager generates a frequency adjusted clock signal that is synchronized with the output clock signal during concurrence periods. The digital clock manager includes a delay lock loop and a digital frequency synthesizer. The delay lock loop generates a synchronizing clock signal that is provided to the digital frequency synthesizer. The output clock signal lags the synchronizing clock signal by a DLL output delay. Similarly, the frequency adjusted clock signal lags the synchronizing clock signal by a DFS output delay. By matching the DLL output delay to the DFS output delay, the digital clock manager synchronizes the output clock signal and the frequency adjusted clock signal.